UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/564,856	01/17/2006	Yasushi Inagaki	283026US90PCT	5109

22850 7590 10/04/2010

OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
PATEL, ISHWARBHAI B	
ART UNIT	**PAPER NUMBER**
2841	

NOTIFICATION DATE	DELIVERY MODE
10/04/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com
oblonpat@oblon.com
jgardner@oblon.com

Office Action Summary	Application No.	Applicant(s)	
	10/564,856	INAGAKI ET AL.	
	Examiner	Art Unit	
	Ishwarbhai B. Patel	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 19 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 January 2006* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/24/10;6/8/10, 3/16/10*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 17, 2010 (along with the preliminary amendment filed on August 19, 2010) has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 3 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Strandberg (US Patent No. 6,323,435) in view of Westbrook (US Patent No. 6,203,967), Tsukada (US Patent No. 6,809,415), and Cooray (US Patent No. 6,749,927).

Regarding claim 1, Strandberg in figure 1-3 discloses a multilayer printed wiring board comprising: a core substrate (12) having a first surface and a second surface on

an opposite side of the first surface (see figure); a plurality first conductive layers formed on the core substrate (conductive layer on the upper surface, lower surface see figure) respectively, and comprising one of a power source layer and a ground source layer (layer on the core layer is considered as ground conductor, as obvious to use the conductive structure as a power or ground conductor depending upon the requirement); an interlayer insulation layer (30) formed on the first conductive layer (conductive layer on the upper surface) and the core substrate and a second conductive layer (36) formed on the interlayer insulation layer, wherein the first conductive layer on the core substrate are plane layers formed on the first and second surface of the core substrate, respectively (the conductive layers are formed on the plane surface. Also, it is known in the art and obvious to a person of ordinary skill in the art to form the power / ground layers with comparatively larger areas to avoid power loss), and has a thickness which is larger than a thickness of the second conductive layer on the interlayer insulation layer (the invention is for very thin build up wiring layer, column 3, line 5-65, explained in more detail in the parent case, Westbrook, figure 3A-3B, column 8, line 1-10, surface layer with a thickness of 20-40 microns and build up layers are 5-10 micron thick), and the first conductive layer on the core substrate has a side face which is tapered, such that an angle, θ, formed by a straight line connecting the top end and bottom end of the side face of the conductive layer and a horizontal face of the core substrate (see figure 2, shown in more detail).

Strandberg does not explicitly disclose the angle, θ, satisfies $2.8<\tan\theta<55$.

Tsukada in figure 2A discloses a circuit board with the conductive layer (3) having a taper angle with the tanθ about 7 (column 4, line 25-35) and further recites that this will help in better adhesion between the substrate and the conductive layer (column 1, line 25-40).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the board of Strandberg with the angle θ meeting the limitations as recited in the claim, as taught by Tsukada, in order to improve the adhesion between the substrate and the conductive layer.

Further, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Further, Strandberg discloses the interlayer insulation layers on only one side of the core board (upper side). However, interlayer insulation layers formed on both the sides of the core layer is old and known in the art, which will increase the wiring density. Cooray in figure 1 discloses a circuit board structure on both the sides of the core substrate.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time applicant's invention to provide the modified board of Strandberg with the interlayer insulation layers formed on both the sides of the core layer, as taught by Cooray, in order to increase the component density. This modified structure will meet the claimed limitation of plurality of the interlayer insulating layers formed on the first conductive layer respectively.

Regarding claims 2 and 3, the modified board of Strandberg further discloses the thickness of the first conductive layer on the core substrate is α1, the thickness of the second conductive layer on the interlayer insulation layer is α 2, and the α1 satisfies relation of α 2< α1<40 α2, (claim 2) and discloses the thickness of the first conductive layer on the core substrate is α1, the thickness of the second conductive layer on the interlayer insulation layer is α 2, and the α 1 satisfy a relation of 1.2 α 2 < α 1<40 α 2, (claim 3) [the range of thickness as applied to claim 1 above, meets the limitation].

Further, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Regarding claim 19, the modified board of Strandberg further discloses a via hole (34) formed in the interlayer insulation layer and electrically connecting the first conductive layer on the core substrate and the second conductive layer on the interlayer insulation layer.

4. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over the modified board of Strandberg as applied to claim 1 above, and further in view of Lykins (US Patent No. 6,440,641).

Regarding claim 20, Strandberg discloses all the features of the claimed invention as applied to claim 1 including the first conductive layers on the core substrate

but does not explicitly disclose the conductive layers comprise a copper foil, an electroless plated film and electrolytic plated film. However, to start with a thin foil / film and to increase the thickness to desired value with electroless plating and subsequent electrolytic plating is old and known in the art. Lykins in figure 6A discloses a circuit board structure with the layer formed on the core layer is formed by plating process on the initial copper foil (column 6, line 60 to column 7, line 5. Though electroless plating is not explicitly described, it is there for better subsequent electrolytic plating).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the modified board of Strandberg with the conductive layers comprise a copper foil, an electroless plated film and electrolytic plated film, as taught by Lykins, in order to have desired thickness of the conductor.

Response to Arguments

5. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) / explanation of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kanechika (US Patent No. 6,434,818) in figure 2 and 4 discloses a conductive layer (pattern) with tapered side face.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwarbhai B. Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jinhee Lee can be reached on (571) 272 1977. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ibp
September 26, 2010

/Ishwarbhai B Patel/
Primary Examiner, Art Unit 2841